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PATENT, TRADEMARK
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24956

PATENT, TRADEMARK OFFICE

10/086718
U.S. PTO
03/04/02

To: Assistant Commissioner for Patents
Washington, D.C. 20231

Sir: Transmitted herewith for filing is the patent application of:

Inventor: H. MIYAGAWA et al (See Attached List)

For:
MODULATION SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
AND TESTING METHOD FOR OSCILLATION CIRCUIT

Enclosed are:

☒ 9 Sheets of Drawings

This application is being filed without an executed Declaration.

Priority is claimed from Japanese Application No. 2001-158823
filed May 28, 2001. ☐ A certified copy is attached herewith.
Copies of the disclosure documents listed on the attached PTO 1449 form and
☐ discussed in the specification or ☐ attached Information Disclosure Statement.

A verified statement to establish small entity status under 37 CFR 1.9 and 1.27.

Specification: Abstract ☒ Description 34 pages; and 10 claim(s).

☒ Preliminary Amendment.

☐ Executed Declaration.

The filing fee is calculated as shown below:

Small Entity

Large Entity

For:	No. Filed	No. Extra
Basic Fee		
Total Claims	10 - 20 = *	0
Indep Claims	2 - 3 = *	0
<input type="checkbox"/> Multiple Dependent Claim (s)		

* If difference is less than zero
then enter '0' in second column

Rate	Fee
	\$ 370
x 9	\$
x 42	\$
+ 140	\$
Total	\$

OR

Rate	Fee
	\$ 740
x 18	\$ 0
x 84	\$ 0
+ 280	\$ 0
Total	\$ 740

☒ A check in the amount of \$ 740.00 is enclosed for the filing fee.

☒ The Commissioner is hereby authorized to charge any additional fees that may be required to Deposit Account No. 50-1417.

Respectfully Submitted,

By:

John R. Mattingly
Registration No. 30,293

1132 U.S. PTO
03/04/02

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